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1 **A novel CMOS compatible multi-level flash EEPROM for embedded applications**

Concannon, A.; McCarthy, D.; Mathewson, A.; Guillaumot, B.; Papadas, C.; Kelaidis, C.;

Device Research Conference Digest, 1998. 56th Annual, 22-24 June 1998
Pages:78 - 79[\[Abstract\]](#)[\[PDF Full-Text \(364 KB\)\]](#)

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2 **High performance SONOS memory cells free of drain turn-on and over-erase: compatibility issue with current flash technology**

Myung Kwan Cho; Kim, D.M.;

Electron Device Letters, IEEE, Volume: 21, Issue: 8, Aug. 2000
Pages:399 - 401[\[Abstract\]](#)[\[PDF Full-Text \(52 KB\)\]](#)

IEEE JNL

3 **Fast and accurate programming method for multi-level NAND EEPROMs**

Hemink, G.J.; Tanaka, T.; Endoh, T.; Aritome, S.; Shirota, R.;

VLSI Technology, 1995. Digest of Technical Papers. 1995 Symposium on, 6-8 June 1995

Pages:129 - 130

[\[Abstract\]](#)[\[PDF Full-Text \(180 KB\)\]](#)

IEEE CNF

4 **Functionally separated, multiple-valued content-addressable memory and its applications**

Hanyu, T.; Aragaki, S.; Higuchi, T.;

Circuits, Devices and Systems, IEE Proceedings [see also IEE Proceedings G-Circuits, Devices and Systems], Volume: 142, Issue: 3, June 1995

Pages:165 - 172

[\[Abstract\]](#)[\[PDF Full-Text \(516 KB\)\]](#)

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5 **Variable stress-induced leakage current and analysis of anomalous charge loss for flash memory application**

Yamada, R.; King, T.J.;

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1 Multiple-valued floating-gate-MOS pass logic and its application to logic-in-memory VLSI

Hanyu, T.; Teranihi, K.; Kameyama, M.;

Multiple-Valued Logic, 1998. Proceedings. 1998 28th IEEE International Symposium on , 27-29 May 1998

Pages:270 - 275

[\[Abstract\]](#)
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2 A floating-gate-MOS-based multiple-valued associative memory

Hanyu, T.; Higuchi, T.;

Multiple-Valued Logic, 1991., Proceedings of the Twenty-First International Symposium on , 26-29 May 1991

Pages:24 - 31

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3 Multiple-valued logic-in-memory VLSI based on a floating-gate-MOS pass-transistor network

Hanyu, T.; Teranishi, K.; Kameyama, M.;

Solid-State Circuits Conference, 1998. Digest of Technical Papers. 45th ISSCC 1998 IEEE International , 5-7 Feb. 1998

Pages:194 - 195, 437

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4 Design of a high-density multiple-valued content-addressable memory based on floating-gate MOS devices

Hanyu, T.; Higuchi, T.;

Multiple-Valued Logic, 1990., Proceedings of the Twentieth International Symposium on , 23-25 May 1990

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5 Design of a one-transistor-cell multiple-valued CAM

Hanyu, T.; Kanagawa, N.; Kameyama, M.;